## REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated March 13, 2007. In addition, a Request for Continued Examination is being submitted concurrently herewith. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 2 and 4-9 are under consideration in this application. Claim 3 is being cancelled without prejudice or disclaimer. Claims 2 and 4-7 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention. New claims 8-9 are being added.

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims and the specification are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The drawings were objected to for not showing reference signs described in the specification, and the specification was objected to for informalities. Applicants hereby defer submitting the corrected drawings and the substitute specification until such time as the Examiner indicates the presence of allowable claims in this application.

Claims 2, 5, 7 were objected for informalities, and claims 2-7 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Since claim 3 is being cancelled without prejudice or disclaimer, and claims 2 and 4-7 are being amended as required by the Examiner, the withdrawal of the outstanding informality objection and rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 2-7 were rejected under 35 U.S.C. §103 (a) as being unpatentable over the newly cited reference US Pat. No. 6,279,146 to Evans et al. (hereinafter "Evans") in view of

US Pat. No. 6,564,367 to Fujii et al. (hereinafter "Fujii"). This rejection has been carefully considered, but is most respectfully traversed.

The logic verification system of the present invention, as now recited in claim 2, comprises a logic simulation accelerator (Figs. 1-4 and 6) which includes a logic simulator 0010 (in Fig. 4 or 0096 in Fig. 16) operating on a general purpose processor 0013 to **logically verify operation correctness of a designed logic circuit** ("*the designed logic circuit is verified using a system called the logic simulator having the function to verify the operations by artificially operating the logic circuit of the step S0102 on the general purpose processor*" [0036] of corresponding US. Pub. No. 2004/0078179; "*logical verification (logical simulation)*" Step 0103 in Fig. 1); a device 0027 which includes a programmable [[EPGA]]FPGA module composed of FPGAs to be programmed to **physically realize functions of the designed logic circuit** ("*proto-typing (logical emulation)*" Step 0106 in Fig. 1; [0095]-[0096]) and which is mounted to the logic simulator 0010 via a connecter (e.g., 0039) ([0059]; [0083]; Figs. 2 and 12); a bridge circuit 0011 which is mounted to the logic simulator 0010 and which selectively transmits and receives corresponding data between said general purpose processor 0013 and said device 0027 (Fig. 4; paragraph 0060, 0061, 0065 and 0067; [0085]). All pins of the FPGA module are wired directly to the bridge circuit via the connector ([0095]). A cutting end of **a verification logic which verifies said designed logic** circuit **realized on said device 0027** is assigned to the connector of the FPGA module for accelerating logic simulation ([0096]). A correspondence between each of said all pins of said FPGA module and a logic signal from said general purpose processor is established on said logic simulator ([0096]). The verification logic for verifying said designed logic circuit realized on said device 0027 provides a means 0053-0056 for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit 0011 thereby performing **logic verification of the designed logic circuit** by the logic simulator 0010 in parallel with **physical realization of the designed logic circuit one said device 0027 (Fig. 1, [0038])**, and said direction control signal is sent to the bridge circuit 0011 via one of said two-way signals ([0038]; Fig. 1; [0055]; "*the direction control signal of two-way signal is added to the logic as the port or the pins of connector of the FPGA module and it is then transmitted to the logic simulator side*" [0101]; Figs. 17-19).

"*As specified in the step S0106, the logic emulation is performed using a programmable device such as the PFGA in parallel with verification by logic simulation,*

*logic synthesizing and layout from the timing near the end of verification by the logic simulation. This verification is intended to operate the logic at the rate near to the actual operation through combination with actual peripheral components by programming the logic which is designed as the programmable device, detect specification error of actual components and extract, before manufacturing of LSI, failure on the case where execution is impossible in the logic simulation because a verification pattern is very longer* ([0038])." *"The logic simulation accelerator of this embodiment executes the logic simulation program on the disk memory 0014 on the general purpose processor 0013. The bridge circuit 0011 transmits and receives the simulation object logic indicated by hardware on the FPGA and the signal via the general purpose interface to realize the simulation of verification object logic. When the FPGA module 0010-1 is not provided, artificial operation of the verification object logic which must be executed with the general purpose processor 0013 is actually operated as the logic indicated by the hardware on the FPGA. Thereby, the processing rate can be accelerated by reducing the number of processes to be executed with the general purpose processor 0013 ([0063])."*

"*Switching of mode enables that the intrinsic logic operation is executed during logic emulation, while the direction control signal of two-way signal is transferred to the bridge circuit with correspondence to the two-way signal without increase of pins when the logic simulation is accelerated* [0104]."

"T*he function regarding the signal (re) enables that when the operation to transfer, on the time division basis, the direction control signal of two-way signal and the two-way signal itself is selected, the transmission timing of the two-way signal and direction control signal is transmitted to the FPGA module from the bridge circuit, and the two-way signal and direction control signal are respectively transmitted to the bridge circuit depending on change of the signal* [0105]."

As recited in claim 6, a disagreement between the signal direction of the two-way signal to the logic simulator and a signal direction indicated in said direction control signal is detected by comparing said signal directions ([0109]). As recited in claim 8, said direction control signal is added into the verification logic (Fig. 17; [0102]). As recited in claim 9, said direction control signal is instead transmitted on a time division basis with said two-way signals (Fig. 18; [0103]).

Applicants respectfully contend that the cited references do not teach or suggest such "a logic simulator + EPGA module ***parallel*** logic verification scheme which including a logic

simulation program operating on a general purpose processor to **logically verify operation correctness of a designed logic circuit** working in parallel with an EPGA module 0027 composed of FPGAs programmed to **physically realize functions of the designed logic circuit**, and a means 0053-0056 for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit directly connected to all pins of the said FPGA module thereby performing **logic verification of the designed logic circuit** by the logic simulator 0010 in parallel with **physical realization of the designed logic circuit one said device 0027**" as does the invention.

As admitted by the Examiner (p. 6, paragraph no. 19 of the outstanding Office Action), Evans does not teach "all pins of the FPGA module being directly wired to the bridge circuit, a cutting end of a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module, and a correspondence between each pin of the external interface connector of said FPGA module and a logic signal is established on said logic simulator on said general purpose processor."

In addition, as shown in Fig. 6, Evans executes emulation, i.e., physical realization of the designed logic circuit (box 318) on it own, rather than "in parallel with logic verification of the designed logic circuit (Fig. 1)" as does the present invention. Evans also does not provide "means 0053-0056 for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit directly connected to all pins of the said FPGA module thereby performing" the ***parallel*** logic verification scheme of the present invention.

Fujii was relied upon by the Examiner to provide teachings missing from Evans. However, Fujii shares the above-mentioned deficiencies as Evans. As shown in Fig. 25, Fujii also executes emulation, i.e., physical realization of the designed logic circuit (S2505) on it own, rather than "in parallel with logic verification of the designed logic circuit (Fig. 1)" as does the present invention. Fuji merely uses a general purpose processor to divide a target logic circuit into different FPGAs, but not to execute a logical simulation, much less of executing such a logical simulation in parallel with the FPGA module as the present invention.

Fujii also does not provide "means 0053-0056 for transmitting a direction control signal which controls a transmission direction of two-way signals between said FPGA module and said bridge circuit directly connected to all pins of the said FPGA module thereby performing" the ***parallel*** logic verification scheme of the present invention.

Lastly, the features recited in claims 4-9 are simply absent from the disclosures of Evans or Fujii.

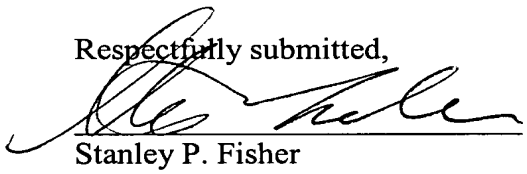
The cited prior art references and their combinations all fail to teach or suggest each and every feature of the present invention as recited in independent claim 2 and it dependent claims. As such, the present invention as now claimed is distinguishable and thereby allowable over the prior art references cited in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and telephone number indicated below.

Respectfully submitted,



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**July 11, 2007**

SPF/JCM/JT